Tirna Electronics

Switched Capacitor Filter (SCF) Module

- 10th Order Root Rasied Cosine Low Pass

This module, which is shown in fig. 1, is based on the Linear Technology Corporation LTC1569 linear phase, DC accurate, tuneable, low pass SCF. This chip implements a 10th order root raised cosine response, combining good selectivity with linear phase in the pass-band and making it ideal for a range of applications including communications and data acquisition systems. See www.linear.com for a full datasheet on the LTC1569-7. We strongly recommend reading this datasheet in addition to the data on our module.

Features

- Single 11-turn variable resistor and jumpers set cut-off frequency.
- External clock input facility via jumpers.
- 10th order, linear phase, root raised cosine, response.
- Jumper selectable single sided or dual supply options.
- Operates from 3V to ±5V
- Over 300 kHz cut-off frequencies achievable on ±5v supplies ($I_{supply} \leq$ 33mA).
- Up to 300 kHz cut-off frequency on single 5v supply ($I_{supply} \leq$ 22mA).
- Up to 150 kHz cut-off frequency on single 3v supply ($I_{supply} \leq$ 10mA).
- DC accurate, typical V_{os}(max) = 5mV.
- Differential or single-ended inputs.
- Operating Temperature range 0 to 70˚ C

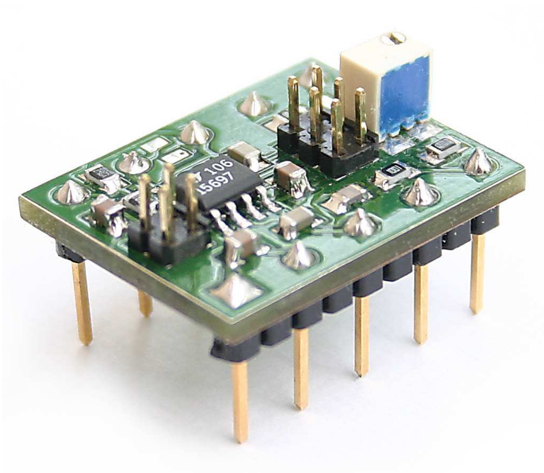

Figure 1: Tirna Electronics SCF Module

Why Root Raised Cosine?

Root raised cosine filters were originally designed for application in communications links where the filtering which defines the channel amplitude/frequency response is split equally between the transmitter and receiver ends of the link. The root raised cosine filter at the transmitter end of the link being used to limit the spectral bandwidth of the baseband (information signal) and the identical root raised cosine filter at the receiver end being used to implement a frequency matched filter, maximising signal-to-noise ratio at the receiver baseband output. Having a root raised cosine filter at each end of the link gives an overall raised cosine shape to the amplitude/frequency response of the channel which, according to the Nyquist vestigial symmetry theorem, should give zero inter-symbol interference between adjacent digits.

However, root raised cosine is not just for communications applications. Linear phase in the pass-band combined with a sharp cut-off beyond the pass-band edge make it ideal for general filtering applications including data acquisition.

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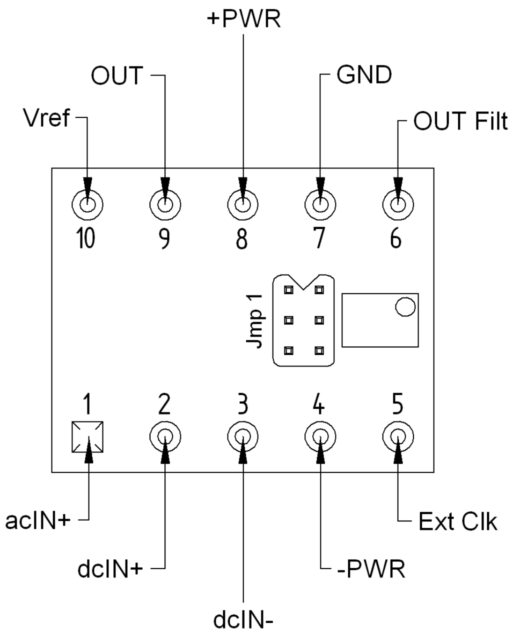
Switched Capacitor Filter Module - 10th Order Root Raised Cosine, Low Pass

Pin layout



Pin 1: A/C coupled signal input, IN+

Pin 2: D/C coupled signal input, IN+

Pin 3: D/C coupled signal input, IN-

Pin 4: -3V to -5V (double sided supply)
0V (single sided supply)

Pin 5: External square wave clock I/P

Pin 6: Filtered output (1st order RC filter to reduce clock feed-through – R & C components may need changing depending on clock frequency. Changes require surface mount soldering capability).

Pin 7: Ground

Pin 8: +3V to +5V power supply

Pin 9: Unfiltered SCF output (clock feed-through unattenuated)

Pin 10: V_{ref} in/out. This pin is connected internally in the LTC1569 chip to the center point of a resistive divider chain comprising 2, 14kΩ resistors across +PWR and –PWR. Thus on double sided supplies this pin will have a nominal value of 0V. Since the internal voltage on this pin is from a 7kΩ source impedance, this pin can be connected to an external reference voltage (assumed zero impedance) which would then become the reference voltage for the output waveform.

How to Set-up the Module

Set the corner frequency of the filter (assumed here to be the -3dB frequency of the filter) to the desired method as follows:

1. Decide whether you are going to use a double sided power supply (±3V to ±5V) or a single sided supply (0/3V to 0/5V) with the SCF module.

2. Decide whether you will use the on-board (internal) clock or an external clock and set the appropriate jumper on JMP1 (see below).

3. Power up the module so that it will have power applied to it before you connect an input. This is a good basic rule with CMOS devices as it reduces the probability of latch-up (often fatal for CMOS as it leads to a short circuit across the supplies internal to the chip).

4. Set a sinewave generator to a frequency equal to one tenth of the desired corner frequency of the filter. Adjust the amplitude of the generator to be 1V peak-to-peak and connect its output using co-axial cables and a "T" piece to both inputs of a dual beam oscilloscope switched to 200mV / cm. You should get 2 sinewaves 5 cm peak-to-peak. Adjust the gain trim settings of one of the scope channels, if necessary, to achieve the same amplitude of signal on each beam and adjust the generator output amplitude for 5cm peak-to-peak on both beams.

5. Remove one coaxial cable from the oscilloscope and generator, and use a cable to connect the signal generator to the filter module AC input (Pin 1). Using the AC input saves having to think about the DC value of the generator's output at this stage, but remember that this input is -3dB at 1.3Hz so will cause attenuation below about 5Hz. When using the AC input, ensure that Pin 3 of the module is tied to pin7 if using double sided supplies, or pin10 in the case of single sided supplies.

6. Observe the output of the filter module on the second channel of the oscilloscope. The non-reconstructed output can be found on Pin 9 of the module.

7. With a small screwdriver, adjust the clock frequency of the module so that the corner frequency is at least a decade above the generator input frequency. When this has been achieved, the input and output amplitudes of the filter module should be the same (i.e. 1V peak-to-peak).

8. Adjust the generator output frequency to the desired corner frequency of the filter (assumed here to be defined as its -3dB (1/2 power) frequency, (F_c)).

9. Again using a small screwdriver, adjust the 11 turn, 50k Ohm variable resistor which sets the clock frequency the filter module until the output amplitude of the filter is 0.71 times the input amplitude($0.71 \approx 1/\sqrt{2}$ = -3dB = 1/2 power). The input amplitude should still be 5 cm peak-to-peak on the oscilloscope screen. This means that the amplitude of the output of the filter module should have dropped to 3.5 cm peak-to-peak. The filter is now set-up to the desired corner frequency, F_c.

10. Test the amplitude/frequency response of the filter from $0.1F_c$ to $10.0F_c$, checking the following points on Table 1 below:

Frequency (Fc)	Input amplitude	Output amplitude	Gain (20Log(Vo/Vi))
0.1 Fc	1V	1.00V	0dB
1.0 Fc	1V	0.70V	-3dB
1.5 Fc	1V	1.4mV	-57dB
2.0 Fc	1V	1.0mV	-60dB

Table 1: *Some important "spot check" frequencies for the LTC 1569 based SCF module.*

You may find it difficult to verify the small outputs at 1.5Fc and 2.0Fc without using a pre-amplifier in front of the oscilloscope input. If you do use a pre-amplifier make sure its gain x bandwidth product (GBP) is adequate. i.e. 2.0Fc x pre-amp gain < ¼ GBP.

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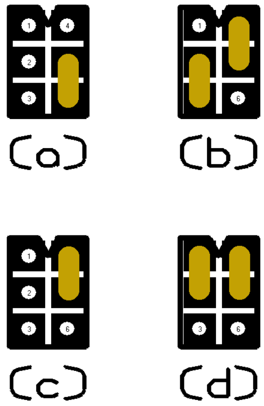
Jumper Settings

Jmp1 Settings:

When using the module's internal clock, Jmp1 allows the user to select from three overlapping ranges of cut-off frequencies. These ranges vary slightly, depending on what supplies are being used, and are illustrated in the following diagrams. Fine tuning of the cut-off frequency is achieved by adjusting the 11 turn variable resistor.



(a) External Clock
(b) Internal Clock Divide by 1
(c) Internal Clock Divide by 4
(d) Internal Clock Divide by 16

±5v Supplies

Internal Clock	Possible Cut-off Frequency (Hz)
÷16	2K → 25K
÷4	8K → 100K
÷1	32K → 310K

+5v Supply

Internal Clock	Possible Cut-off Frequency (Hz)
÷16	2K → 18K
÷4	8K → 70K
÷1	32K → 300K

+3v Supply

Internal Clock	Possible Cut-off Frequency (Hz)
÷16	2K → 10K
÷4	8K → 40K
÷1	32K → 130K

$$f_{cut\text{-}off}(Hz) = \frac{128{,}000 \cdot \left(\dfrac{10{,}000}{R_{ext}}\right)}{1\ ,\ 4 \text{ or } 16}$$

Where, R_{ext} is in Ω, and is adjusted via the 11 turn variable resistor. The maximum value of R_{ext} is 40kΩ and the minimum value is 3.9kΩ.

These are the maximum and minimum values of R_{ext} recommended by the Filter IC manufacturer and only applies while using +5v or ±5v supplies. If 3v or ±3v supplies are being used, then R_{ext} should lie between 40kΩ and 8kΩ.

As a result, this switched capacitor filter module range has been set to the wider limits of the +5v or ±5v supplies. Care must be taken to ensure that the lower limit is not exceeding while using 3v or ±3v supplies. The value of R_{ext} can be checked at any time by removing the Internal/External Clock jumper in Jmp2, and measuring the resistance between Pin 8 (V+) of the filter module and the pin of jumper Jmp1 that is closest to Pin 6 (Filtered Output) of the module. A suitable multimeter is required to verify this operation.

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Removal of Clock Feed-Through

The Tirna Electronics SCF Module allows for the provision of an optional on-board RC 1st order filter to help reduce the clock feed-through from the LTC1569-7 Switched Capacitor Filter IC. The -3dB frequency of this RC filter should be 2 octaves above the -3dB frequency of the SCF module. The pads are laid out for an 0805 sized surface mount resistor and capacitor. The filtered output can then be taken from pin6 of the SCF module. The pads for the resistor are located between pins 8&9 while the capacitors pads are situated between pin6 and the variable resistor.

If you are unsure about designing this 1st order RC filter or would like to discuss this with us then please don't hesitate to get in touch.

Anti-aliasing Filter

Input continuous time filters are required to control aliasing at the input to the SCF module. Typically, these filters only need to be 2nd or 3rd order continuous time filters and if your requirements are really modest, you may even only need 1st order filtering. It all depends on the application and on the SCF cut-off frequency to sampling frequency ratio (64:1 for the LTC1569-7 and 128:1 for the LTC1569-6). The higher this ratio, the easier it is to control the amplitude of aliased components.

Butterworth, Continuous Time, Anti-alias, Filter with fc = 4*Fc of the SCF				
Anti-alias filter order	LTC1569-7 (Fs/Fc = 64:1)		LTC1569-6 (Fs/Fc =128:1)	
	Attn (dB)	V_{out} (mV) (V_{in}=1V)	Attn (dB)	V_{out} (mV) (V_{in}= 1V)
1st	-24.1	62.4	-30.1	31.3
2nd	-48.1	3.9	-60.1	1.0
3rd	-72.2	0.25	-90.2	0.03

Table 2: *Attenuation of aliased components close to Fs for 1st, 2nd & 3rd order Anti-alias filters with corner frequencies 2 octaves above the SCF corner.*

Anti-aliasing Filters – Own Design

If you want to design your own anti-aliasing filters but need some guidance, read our tutorial article on the subject.

Anti-aliasing Filter Design Service

If you wish, we can do the design, or the design, build and test of your anti-aliasing filter. We have off-the-shelf, 3rd order, continuous time, low-pass filter modules in an 8-pin DIL outline. We just need to know the required cut-off frequency. Please fill in the quote request form for a free quote.

If you wish, you can also purchase these modules minus the components that define the cut-off frequency. This will allow you to solder your own 0805 case components onto the module as you wish. To enable you to work out the component values, you may wish to download filter design software from the Texas Instruments website. Please feel free to e-mail for advice or help.

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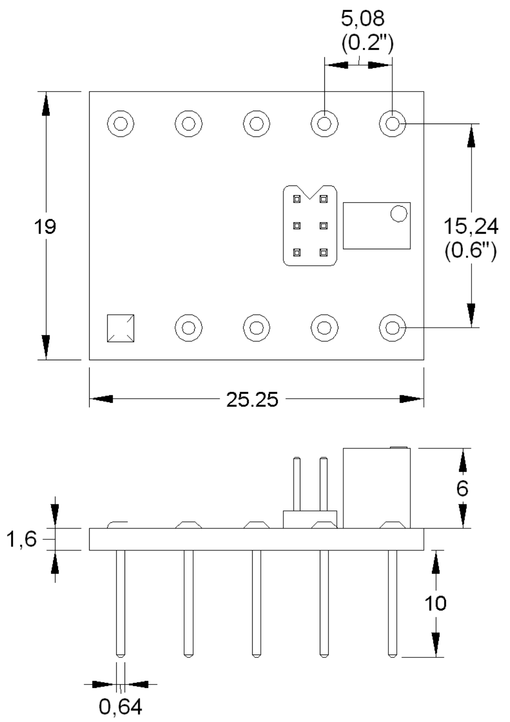
Electrical Specs

Dimensions

Dimensions are shown in millimetres unless otherwise stated.



Board:

Dimensions	25.25 x 19 mm
Material	FR4
Thickness	1.6mm
Copper Thickness	35µm (1oz)
Finish	Green Soldermask

Pins:

Material	Phosphor Bronze
Finish	Tin on Nickel
Length (below board)	≈10.00mm
Height (above board)	≈0.5mm
Diameter	0.64mm Square

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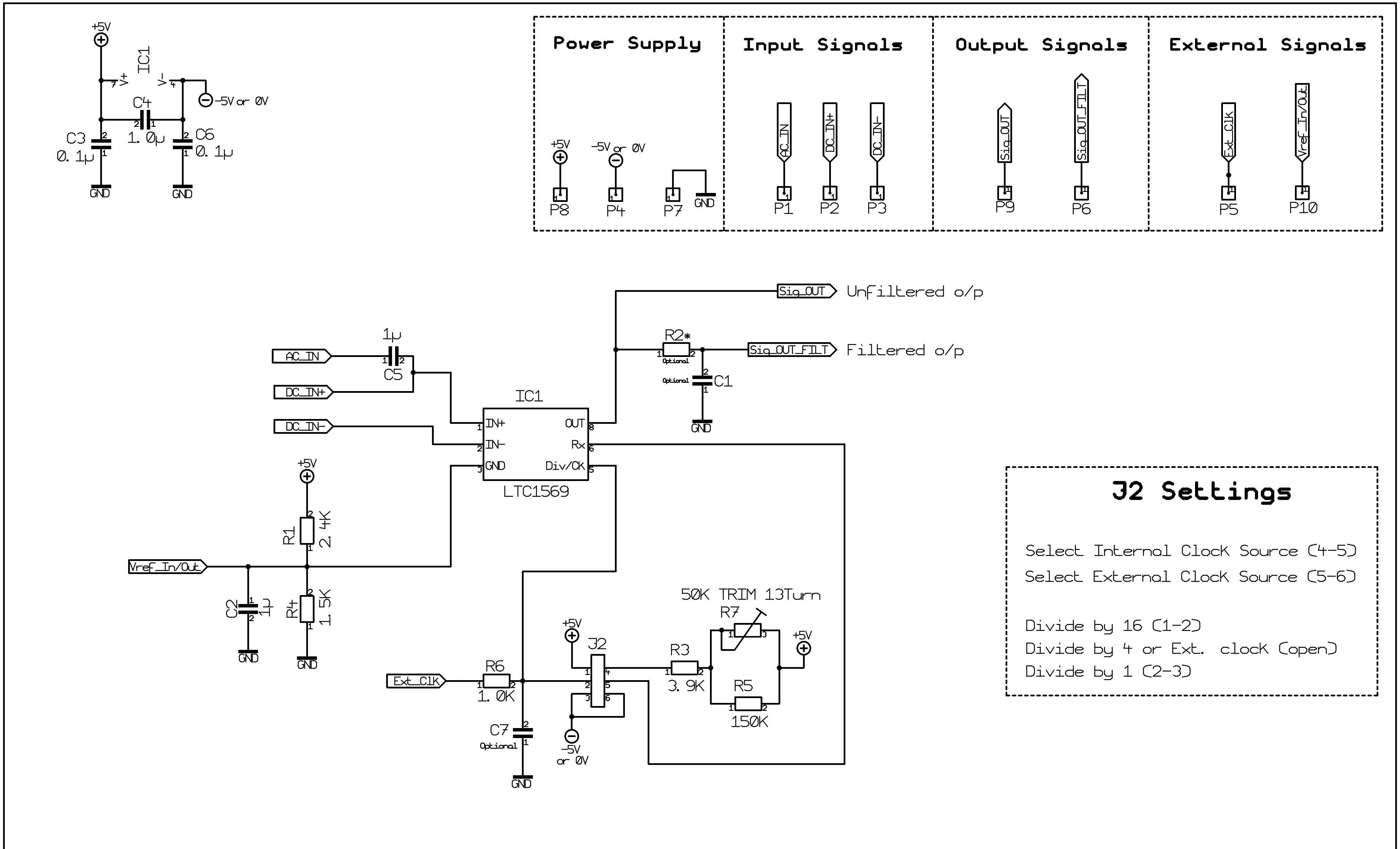

Notes:

* R2 and C1 form an optional 1st order Low Pass Filter to reduce clock feed-through.
The -3dB frequency of this RC filter should be 2 octaves above the -3dB frequency of the SCF module

** The minimum and maximum resistances of the frequency tuning circuit are:
MIN = 3.9KOhm / MAX = 40KOhm (8KOhm MIN on 3V)

Scale	Date		
76.00% - A4	15/11/05	Tirna Electronics Ltd. www.tirnaelectronics.co.uk	3 Roderick Place West Linton, Peeblesshire Scotland - EH46 7ES
Title: 10th order SC LPF (root raised cosine)			
Project: Switched Capacitor	Schematic Issue: C	Drawn By: Jimmy Dripps	Sheet: 1of1

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